REMARKS

An Office Action mailed November 27, 2007 rejected claims 1-25, 44-46, 48-82 and 100-101. Applicant thanks the Examiner for allowing claims 83-99 and 102-118.

Examiner Interview

Applicant thanks Examiner Tran and SPE Chin for the courtesies extended during the telephonic interview with Karl Bizjak (inventor) and the undersigned on February 18, 2009. In the interview, Applicant explained that the synchronous counter of Kitani does not perform the functions of the synchronizer recited in claim 1. Applicant also explained that the low pass filter of Kitani is incapable of detecting a condition that includes one of a zero crossing and failure to have a zero crossing and, consequently, Kitani does not teach an input detector for detecting a predetermined condition of the input signal, wherein the predetermined condition of the input signal includes at least one of a zero crossing and a failure to have a zero crossing within a predetermined period. Examiner and SPE responded that the recitation of the input detector for detecting a predetermined condition was open-ended and predetermined conditions other than zero crossing conditions could be read into the claim. The parties agreed that Applicant will submit amendments to the claims to require detection of zero crossing and failure to have a zero crossing and that Kitani and the other references do no teach such detection or an input detector performing such detection.

Claim Amendments

Taking into consideration the comments of the Examiner at the February 2009 interview, Applicant has amended the claims to more clearly distinguish the claims of the present Application from the art of record. These amendments are submitted to advance prosecution and Applicant maintains that the previously presented claims are patentable; these amendments are submitted to obtain protection of certain specific embodiments of Applicant's invention.

Claim 1 now recites an input detector configured to detect zero crossings of the input signal and failures to have a zero crossing of the input signal within a predetermined period. The art of record does not teach an input detector that can detect both zero crossings and failures to have zero crossings.

Kitani does not teach detection of either a zero crossing or a failure to have a zero crossing. When addressing the requirement for an input detector, the Office Action notes the

presence of rectifier 13 in Kitani and states that the rectifier 13 can detect the presence of a signal; the Office Action states that presence of a signal could be a predetermined condition. Notwithstanding the inability of Kitani's rectifier to perform the functions required in previously presented claim 1, Applicant has amended claim 1 to expressly require the input detector detects both a zero crossing and a failure to have a zero crossing. Kitani's full wave rectifier 13 eliminates zero crossings and has no capability of detecting zero crossings or absences of zero crossings. Therefore, Kitani does not teach an input detector that detects both zero crossings and failures to have zero crossings within a predetermined time as required by amended claim 1.

The amendment of claim 1 removes the necessity for further review of the differences between a synchronizer that synchronizes a gain signal and a synchronous counter driven by a system clock unconnected with an input signal having the properties required by claim 1. Nevertheless, for completeness, Applicant notes that Kitani's synchronous counter receives only two binary digital inputs: an up/down control and a digital clock signal. Neither of these digital inputs is an input signal from which an input detector detects zero crossings and failure to have zero crossings within a predetermined time.

Browder is introduced in the Office Action for the express reason that Kitani does not disclose detecting a predetermined condition of an input signal that includes at least one of a zero crossing or failure to have a zero crossing. Browder does not teach detecting zero crossings in a manner that synchronizes the input signal to a gain signal. Browder teaches essentially the same gain control circuit as Kitani with the exception that the clocking signal of the synchronous counter in Browder is derived from a crossover detector that monitors a signal to be amplified. This crossover detector in Browder controls the rate of change of gain of a variable digital attenuator based on the frequency of zero crossovers. Browder reacts to zero crossings but, if no zero crossovers are present, the output of Browder's counter does not change. Browder does not synchronize a gain signal with an input signal as required in the amended claims, but instead changes (by counting) a gain value only after a zero crossing.

The amendments to claim 1 further distinguish the claimed invention from Browder because Browder does not teach an input detector to detect both a zero crossing and a failure to have a zero crossing.

The Southard is not relevant art. Southard is directed to methods for generating waveforms. The systems and methods described in Southard generate a waveform and Southard

has no teaching, suggestion of detecting a failure to have a zero crossing. Southard's "compander" is an industry standard A-law or micro-law linear to logarithmic bit length compressor. Southard does not support a rejection of any claim in the present Application.

Independent claims 44, 50 and 75 are amended to depend from and further limit claim 1. These amendments are submitted to speed prosecution and may be resubmitted in original form in a continuation application. As discussed above, no combination of the prior art teaches the synchronization of signals based on both a zero crossing and a failure to have a zero crossing.

Independent claim 72 is amended to require a method that provides an output by synchronizing a first signal and a gain signal upon detection of a zero crossing of the first signal, and synchronizing the first signal and the gain signal upon detection of a failure to have a zero crossing of the first signal within a predetermined period. Therefore, the recited method is required to synchronize upon detection of each of two conditions: a zero crossing and a failure to have a zero crossing. As discussed above, no combination of the prior art teaches such synchronization of signals.

Applicant has amended dependent claims 5, 9, 10, 12, 19, 100 and 101 for consistency with amended claim 1. In each of these dependent claims, the amendments reconcile the claim language in elements that refer to a "predetermined condition;" the amendments use more specific recitations of zero-crossing related conditions in place of the predetermined condition (*See, e.g.*, claim 5).

Applicant submits new claims 119 and 120, each of which depends from claim 1 and defines, by limitation, certain specific embodiments of the claimed invention. Claim 119 ties zero crossings to the end of a half wave. Claim 120 ties zero crossings to the end of a half cycle. Claims 119 and 120 are fully supported in the Specification and Drawings and no new matter is added to the Application by this claim addition. Entry of the new claims is requested.

For at least the reasons provided above, Applicant submits that the rejections of the claims are moot and that all claims are patentable over the art of record.

CONCLUSION

All objections and rejections having been addressed, it is respectfully submitted that the present application is in a condition of allowance and a Notice to that effect is earnestly solicited.

As agreed in the interview, the Examiner is requested to contact the undersigned at the (650) 233-4802, should any points remain in issue.

Please charge any fees associated with the submission of this paper to Deposit Account Number 033975. The Commissioner for Patents is also authorized to credit any over payments to the above-referenced Deposit Account.

Respectfully submitted,
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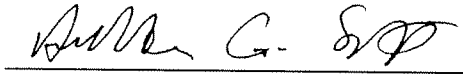

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